# Photoelectrochemical Etching of silicon wafer

## *1-Introduction*

In contrast with electrochemical etching technique just we need a photon source such as lasers and intensive light is used to supply the required holes in the irradiated area of silicon wafer to initiate the etching process. The majority of carriers in an n - type semiconductor are electrons; to generate a sufficient number of holes to carry out the corrosion reaction, the semiconductor must be illuminated. Light generates electron hole pairs near the semiconductor interface, and the built in field sweeps the holes to the surface .

Photochemical etching has been used to produce porous silicon (PS) and nanocrystallites of this way has some drawbacks such as non uniformity of illumination distribution and also the etching process in this method is considered slow . The etching can be performed either in voltage-controlled or in current-controlled mode. The latter is normally preferred, because it supplies the required charge for the reaction at constant rate, regardless of any evolution during etching of the cell electrical impedance, ultimately leading to more homogeneous and reproducible material .

The PS growth is the alignment of the pore nucleation sites along the crystal defects of the Si surface. The defects serve as easy paths for the pore propagation. The dynamic stress during pore growth is another important issue. At the bottom of each pore, the dissolution reaction liberates the essential amount of hydrogen. Outward movement of gas bubbles and products of Si dissolution together with inward propagation of fresh electrolyte are to produce essential hydrodynamic pressure inside

the porous silicon layer. According to the theory of propulsion the essential tensile stresses are produced both in porous silicon and in Si substrates. Therefore, the micro cracks are formed in PS figure (1) and that serve as easy path for further pore growth .

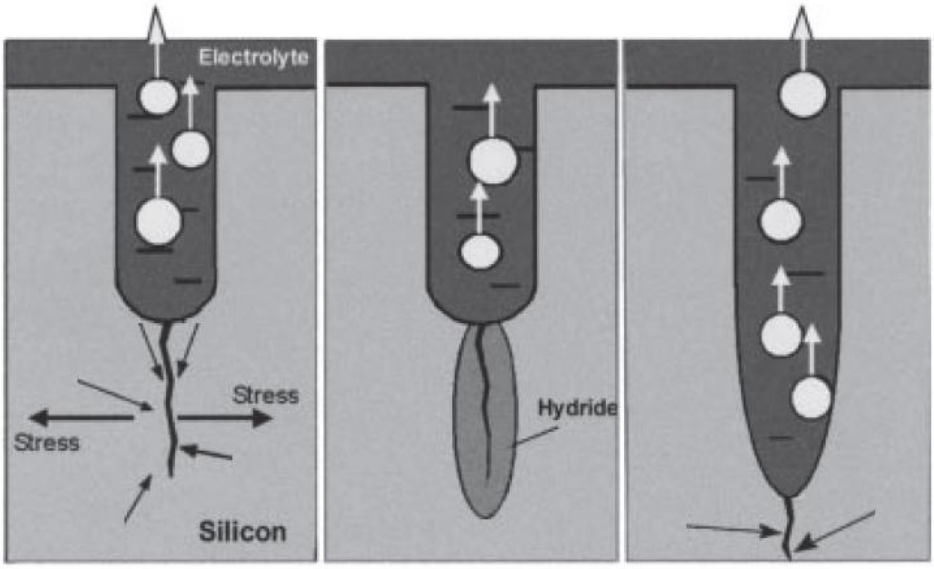



Figure (1): Schematic of the pore growth according to the mechanical stress assisted mechanism of porous silicon

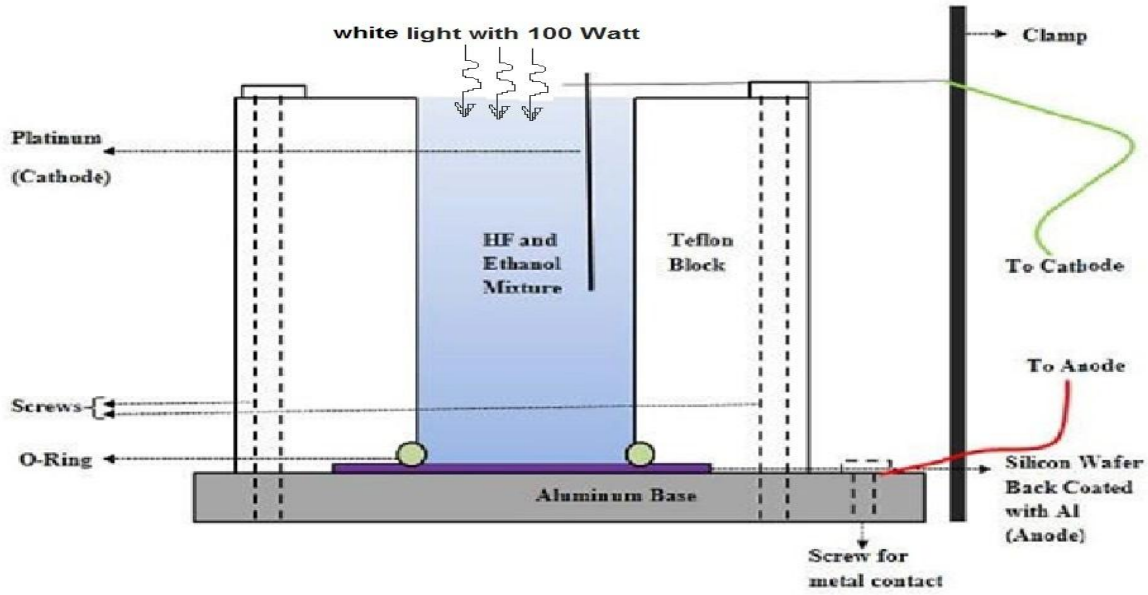
## 2- Substrate Cleaning Steps

The silicon substrates were cleaned by the following steps:

1. They were cleaned using detergent with water to remove any oil or dust that might be attached to the surface of substrate and then placed the slides in cleaning beaker.
2. The beaker contains the cleaning si wafers filled by distilled water and then rinsed in ultrasonic unit for 10 minutes.
3. Step 2 was repeated by replacing the distilled water with pure alcohol solution to remove any organic contaminant and residual particles on it.
4. The substrates eventually were dried by blowing air and wiped with optical soft tissue.

## 3- Preparation of samples

Porous silicon layers are produced using bulk silicon wafers, p-type and n-type, with different resistivities and orientation. Samples are made of porous silicon produced with a standard technique of etching either n or p-type silicon substrates in an electrolyte (40%) HF :( 99.8%) $CH_3OH$ with a volume ratio of like [1:9]. The Si wafer first cuts to (1.2×1.2) $cm^2$ samples before cleaning, Then you put them in the etching cell fig(2) .




Figure(2): Schematic diagram of the porous silicon fabrication system(PEC).

## 3- Questions :

1- Write the etching silicon wafer systems ?
2- Does increasing the etching time always lead to an increase in the thickness of the porous layer?
3- Why is the etching cell made of Teflon?
4- What do you think if we turn the anode instead of cathode of the system, does etching happen?